EE / CprE / SE 491 – sddec20-proj01
PROJECT TITLE：Machine learning for pilot biometrics
Week 9-10 Report

3/15/2020 – 4/12/2020
Client: Rockwell Collins
Point of contact: JR Spidell
Faculty Advisor: Akhilesh Tyagi

Team members:
Jianhang Liu--Data Manipulation SME
Feng Lin--Hardware SME
Xuewen Jiang --- Camera Interface SME
Xiuyuan Guo --- Algorithm SME
Sicheng Zeng - python SME
Junjie Chen --- C code SME
Sicheng Zeng - Team leader

Bi-weekly Summary

For these two weeks, we continue working on improving the algorithm with various techniques like hyper-parameter tuning, quantization, pruning and hardware acceleration.

We made some progress in getting familiar with the xilinx toolsuite and decided which framework we would like to choose for our hardware mapping process. We have also started working on quantizing the pruned model to the tf.lite format. Moreover, we are combining the image pre-manipulation with grid search in order to determine the effect of image pre-manipulation on the structure of CNN model.

Individual Contributions

Xuewen - Due to the bad situation of coronavirus spread worldwide, we cannot get our daughter card (Adapter for MIPI camera) of Ultra 96 that we ordered in March. We are planning to create a new circuit card for the MIPI camera and Ultra 96. We will use PCB123 to create a new schematic and buy the materials we need for the design.

Junjie Chen - I spent some time getting familiar with Xilinx toolsuite. Such as vivado and vitis. I then decided to work on hardware acceleration with some of the existing frameworks like 'Vitis Ai' and 'DNNDK'. Basically still in the process of getting familiar with the tool chain until we apply it with our algorithm.

Feng Lin-Using different FPGA projects to understand mechanisms and keep learning various tools such as Vivado,Vitis. Learn how to load existing BNN FPGA design and load it on our board ulra96. Learn how to accelerate a python function with PYNQ.

Sicheng Zeng- During several weeks, I successfully got the open/close eyes code to a great size and transferred the form from .ipny to .tflite. The finally converted_model is great at size. I also work with a teammate about running the model in the Ultra 96 board. It also successfully got results. I will continue to optimize total latency next week.

Xiuyuan Guo- During this time, I have used the tensorflow to observe the effect of each hyperparameter to the given algorithm and use tensorflow to make a graph to present to the rest of the team.

Jianhang Liu- For the past two weeks, I've tested images with several processing methods to the algorithm and collect data (time cost, accuracy, etc.). Results show that some processing methods do benefit the system but others do not, so it is important to identify the correct way to approach. Besides, I also started to get familiar with PCB123, a PCB design software.

Team Member	Contribution	Hours Worked for the Week	Total Cumulative Hours
Junjie Chen	Built petalinux, ran examples within 'Vitis Ai' and DNNDK	12 h	43 + 12 = 55h
Sicheng Zeng	Transfer the keras open/close eyes code to tensorflow lite and run in an ultra 96 board. Fix several problems about sparsity and frequency number.	12h	8+10+12+ 12+12= 54h
Xuewen Jiang	Create a bill of materials - a spreadsheet in google with a list of parts & review with the team. Download and learn to use PCB123 Use this schematic to create a new schematic & review with the team	10h	6 + 15 + 10+10+10 = 51h

Feng Lin	Learn how to create FPGA to accelerate BNN algorithm, and create different networks using BNN algorithm on github. Try to accelerate python code by using FPGA.	10h	18+ 6 + 4 + 10=38h
Xiuyuan Guo	Change the hyperparameter of the given algorithm and use that to find the best so far to increase the accuracy and decrease latency of algorithm by reduce the layer of the CNN	10h	18+10=28
Jianhang Liu	Tested the algorithm with different image processing methods and collected data, got familiar with PCB 123, the PCB design software, and will help on PCB works.	8h	16+10+6+8 = 40h

Pending Issues

-- The daughter card we build has many limitations such as layers and copper; we need to build it based on our requirements.

Plans

1. Create a block diagram of the daughter card design using draw.io & review with the team.
2. Optimize total latency about the pruned model running on board.